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December 11, 2001

ASSISTANT COMMISSIONER FOR PATENTS
BOX NEW PAT APP
WASHINGTON, D. C. 20231

USPS EXPRESS MAIL
EL 897 676 884 US
DECEMBER 11 2001

Re: NEW PATENT APPLICATION
Attorney Docket No.: 4284
Inventor: Matthias EICHIN et al.
Title: Method for Testing an Integrated Circuit

Dear Sir:

1) I am enclosing a NEW PATENT APPLICATION comprising:

a) 8 pages of specification; 15 claims, 1 independent;
2 Figs. on 2 sheets of formal drawings;
an abstract;
1 return receipt postcard;
b) Declaration, Power of Attorney (Fax Copy);
c) Our Form PTO-2038 in the amount of $780.00 to cover the filing fee **and** the fee for Assignment Recordal. Any fee deficiency or additional fee may be charged to Deposit Account No.: 50-0507;
d) a First Preliminary Amendment;
e) a Second Preliminary Amendment;
f) an Assignment Recordation Form Cover Sheet and one copy of Assignment for Recordal; and
g) an Information Disclosure Statement, Form PTO-1449, 7 references.

2) The Priority of an earlier application:
No. 100 64 478.3, filed on December 22, 2000 in: Federal Republic of Germany is hereby expressly claimed under 35 U.S.C. 119. Please acknowledge the priority claim.

3) This application has been assigned to:
1) Assignee: ATMEL Germany GmbH
Address: Theresienstr. 2
D-74072 Heilbronn
Federal Republic of Germany
and
2) Assignee: Vishay Semiconductor GmbH
Address: Theresienstr. 2
D-74072 Heilbronn
Federal Republic of Germany

The Assignment is being submitted herewith for Recordal.

December 11, 2001

4) The Priority Document will follow.

5) All correspondence for this application is to be sent to: **CUSTOMER NO. 021553.**

Very truly yours,

Walter F. Fasse
Patent Attorney
Reg. No.: 36132

WFF:ar/4284
Encls.: as listed above

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DOCKET NO.: 4284

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE MATTER OF THE PATENT APPLICATION

OF: Matthias EICHIN et al.

USSN: TO BE ASSIGNED

FILED: December 11, 2001

FOR: Method for Testing an Integrated Circuit

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FIRST PRELIMINARY AMENDMENT TO MINIMIZE THE FILING FEE

Dear Sir:

In order to minimize the filing fee, please amend the above identified patent application as follows before calculating the filing fee.

In the Claims:

Please cancel claims **14** and **15**.

Claims **1 to 13** are maintained for calculating the filing fee.

REMARKS:

After calculating the filing fee, please further enter the accompanying Second Preliminary Amendment which adds new claims **16** to **17** for examination.

Respectfully submitted,

Matthias EICHIN et al.
Applicant

By

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WFF:ar/4284
Encls.: postcard

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DOCKET NO.: 4284

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE MATTER OF THE PATENT APPLICATION

OF: Matthias EICHIN et al.

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WASHINGTON, D. C. 20231

December 11, 2001

SECOND PRELIMINARY AMENDMENT

Dear Sir:

After calculating the filing fee, but before the first examination, please amend the above identified application as follows.

In the Claims:

Claims **1 to 13** are maintained unchanged.
Claims **14** and **15** have been cancelled by the First Preliminary Amendment to Minimize the Filing Fee.

Please enter new claims **16** and **17** for examination together with claims **1 to 13**, as follows.

16. (new) Circuit arrangement for performing the method according to claim 1 with an integrated circuit (IC) which

has at least one signal output (OUT), at least one switching element (E1, E2) and at least one circuit unit (SCH),

wherein

the integrated circuit (IC) has a control unit (ST) which is linked to the signal output (OUT) for testing the potential at the signal output (OUT), and

the control unit (ST) is linked to at least one switching element (E1, E2), and

the input of the switching element (E1, E2) is linked to an output of the circuit unit (SCH), and

the output of the switching element (E1, E2) is linked to the signal output (OUT).

17. (new) Circuit arrangement according to claim 16,

wherein

the control unit (ST) for adapting the signals to be tested to the potential of the signal output (OUT) contains an amplifier (LE1, LE2), and

the input of the amplifier (LE1, LE2) is linked to the output of a circuit unit (SCH1),

the output of the amplifier (LE1, LE2) is linked to the input of the switching element (E1, E2),

the control unit (ST) contains at least two comparators (I1, I2 and I3, I4) which form a window discriminator,

and has a logic gate (L1, L2) for performing a logic operation on the test signals (SW1, SW2) and at least one more signal (OS) of the circuit unit (SCH),

the input of the window discriminator is linked to the

signal output (OUT), and

the output of the window discriminator is linked to the input of a logic gate (L1, L2),

the output of the logic gate (L1, L2) is linked to the control input of the switching element (E1, E2), and

the output of at least one logic gate (L1, L2) is also linked to the circuit unit (SCH1) for the selection of defined circuit elements within the circuit unit (SCH1).

REMARKS:

1) Examination of the present application is to proceed on the basis of claims 1 to 13, 16 and 17. Claims 16 and 17 are directly based on original claims 14 and 15 respectively, but omit the original multiple dependencies.

2) Favorable consideration and allowance of claim 1 to 13, 16 and 17 are respectfully requested.

Respectfully submitted,

Matthias EICHIN et al.
Applicant

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WFF:ar/4284
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Method for testing an integrated circuit

BACKGROUND

Field of the invention

The present invention relates to a method for testing an integrated circuit in accordance with the preamble of patent claim 1 and a circuit arrangement for performing this method.

Description of the related technology

In the case of integrated circuits (ICs), electrical measurements are made after the manufacturing process in order to test the circuits. The high degree of complexity makes it necessary to measure not only the output signals of the entire circuit but also the signals of individual internal functional groups of a circuit. In the development phase, additional internal contact surfaces, so-called measuring pads which are assigned to the individual circuit blocks, are integrated for this purpose. Function checks can be performed at these measuring pads provided that the integrated circuits are not yet enclosed in a casing. In the case of the finished integrated circuits, some of the measuring pads are linked to external bond pads for the purpose of checking the correct function, and also in order to measure the signals to be tested at additional output pins even in the assembled state. Both the additional measuring pads within the integrated circuits as well as the additional pins on the finished IC require an additional area which, in the case of miniaturization, increases as a percentage of the whole.

Examples for the previous method are provided by known integrated circuits (IC), such as the U2548 and U2521 from the ATMEL Germany GmbH company, for example. In these cases, a part of the measuring pads present within the integrated circuit was linked to additional measuring pads in order to test signals of individual circuit functions.

Another method working according to the previous state-of-the-art is known from the publication EP 0535776 B1. A test mode is activated at an additional input pin by an available signal and by means of an internal logic in order to thus apply selected signals, which are to be tested, of individual circuit units of the integrated circuit at the additional input pins of the integrated circuit.

The disadvantage of the known methods according to the state of the art is that the areas needed for the function checks occupy a substantial part of the total area of the circuit, particularly in the case of small, but highly integrated circuits, in which the area is divided between the measuring pads within the circuit and the additional pins which are needed for the external measurement of the signals. Because of the large part of the total chip area, this

gives rise to a substantial proportion of the total cost of a circuit. This has a negative effect on profitability, particularly in the case of small circuits which are manufactured in large numbers.

Summary of the invention

The object of the present invention is to provide a method by which the internal signals of an integrated circuit are made available for external function checks with the use of already existing pins. A further object of the invention is to specify a circuit arrangement for implementing the method which can be easily and economically manufactured.

The first-named object of the invention is solved by the features described in patent claim 1. The circuit arrangement is described by the features of patent claims 10 and 11. Favorable embodiments are the objects of the subclaims.

Accordingly, the essence of the invention lies in switching the signals generated by a circuit unit within an integrated circuit, which are not measurable at the outputs in the normal operating mode, as test signals to the existing signal outputs for function checks. To do this, a defined potential value is applied to at least one signal output of the integrated circuit while the supply voltage is available, and the integrated circuit is thus switched into a test mode. A test signal generated by a circuit unit of the integrated circuit is thus applied at the signal output. In order to be able to achieve a reliable switchover into the test mode, it is necessary for the potential value applied at the signal output to be different to the value of the output voltage available at the signal output in normal operation of the integrated circuit. It is particularly advantageous if the potential value is applied or set at the signal output by means of a passive component, for example by a resistor.

In comparison to the previous state of the art, it is advantageous that internal measuring pads do not have to be provided for the individual circuit elements of the circuit unit during the circuit design, and chip area is thus saved. Moreover, no additional pins or thus bond pads are needed for switching the integrated circuit into a test mode or for measuring the test signals. Particularly in the case of integrated circuits with signal outputs which are designed as "open collectors" with "pull up" resistors, a potential value, with which the integrated circuit can be switched into a test mode, can be set in a very inexpensive manner by means of a resistor. Moreover, it is irrelevant to the new method whether or not an input signal is available at a signal input of the integrated circuit. In particular, the output signals of circuit elements of the integrated circuit which is to be tested, which has an oscillator stage for example, can be made available as test signals at the signal output. Moreover, it is also possible to measure the test signal if there is an input signal available at the signal input of

the integrated circuit, in order to check, in particular, the signal processing circuit elements of the circuit unit.

In a development of the method, a plurality of potential values can also be applied at the signal output. By assigning each of the potential values to a different test signal, different test signals can be measured one after the other at a single signal output. In the case of integrated circuits which have only a single signal output, this enables different test signals to be analyzed one after the other at a single signal output with low circuit complexity.

In a development of the method, it is advantageous to test the values of the potential values applied at the signal output for conformity with a reference value by means of a control unit during a defined time window before switching the integrated circuit into the test mode, and to switch the integrated circuit into the test mode in a second time window provided that the potential value available at the signal output corresponds to the defined reference value. In so doing, it is advantageous if the potential value set at the signal output remains constant over time and the test signal represents an alternating voltage. The direct voltage components can thus be easily separated with an external measurement arrangement. In comparison to the previous state of the art, an integrated circuit can be switched into a test mode by means of a single resistor in a particularly simple and inexpensive manner with the method according to the invention.

In the case of a plurality of signal outputs, it is possible in a development of the method for the control unit to test the potential value set at the signal output and apply the test signal at another signal output. The advantages of this are that there is no superimposition with the set direct voltage value and that a direct voltage offset of the test signal can be measured.

In another development of the method, the control unit performs a Boolean logic operation with the potential value set at the signal output and a signal of a circuit component of the circuit unit. An AND logic operation with the negative signal value enables, for example, the integrated circuit to be prevented from being switched into a test mode by a potential available at the signal output. For this purpose, it is advantageous if the logic operation is performed with a control voltage from an output stage of the integrated circuit. This embodiment of the method according to the invention enables the test signal in the test mode to be prevented from being superimposed at the signal output on the output signals available in normal operation, that is if input signals are available for example, in a particularly reliable manner.

Investigations by the applicant have shown that it is advantageous if different test signals are selected as a function of the voltage values set at the signal output, in that, for example,

specific parts of the circuit are activated or deactivated by the control unit when there are defined potential values within the circuit unit. In this manner, defined signal shapes can be generated in the case of the test signals with or without an available input signal.

In a further development of the method according to the invention, the integrated circuit is switched into the test mode if the potential value available at the signal output of the integrated circuit lies within an interval of a window discriminator. In so doing, it is advantageous if the signal heights of the test signals, that is their amplitudes and their direct voltage offsets, are set by means of signal amplifiers so that the direct voltage offset of the respective test signal corresponds to the potential value set at the signal output, and the maximum amplitude of the test signal lies within the interval defined by the respective window discriminator. Crosstalk between adjacent windows of the discriminators can be prevented in this way provided that a plurality of window discriminators are used. Furthermore, the direct voltage value at the signal output is little changed.

The present, new circuit arrangement can be used in an advantageous manner for implementing the method according to the invention. An advantage of the integration of a control unit and at least one switching element according to the second-mentioned object of the present invention is that all internal measuring pads may be eliminated while incurring little additional circuit complexity. Another advantage is that a single resistor, which is connected externally to the signal output, is sufficient to switch the integrated circuit into a test mode if the supply voltage is available.

Brief description of the figures

The method according to the invention is described in the following by means of an embodiment in conjunction with the drawings. They show:

Fig. 1 A first circuit arrangement for implementing the method according to the invention, and

Fig. 2 A second circuit arrangement for implementing the method according to the invention.

Description of the preferred embodiments

The object of the integrated circuit IC shown in figure 1 is to apply the output signals from a circuit unit as test signals to a signal output of the integrated circuit provided that, at the signal output, an externally applied potential value, which can be set by means of an external

resistor for example, corresponds to a defined reference value. The integrated circuit IC has an input pin IN and an output pin OUT for this purpose. The output pin OUT is externally linked to a reference potential RV via a node 100 which is connected to a resistor W1 by means of a switch T1 or to a resistor W2 by means of a switch T2. Furthermore, the integrated circuit has another pin at which a supply voltage VS is available and a pin which is linked to the reference potential RV.

There are two functional units within the integrated circuit IC. The first functional unit contains the circuit functions needed for normal operation of the integrated circuit, which are represented, with the exception of a load element RL connected as a "pull up" between the voltage VDD and a node 50, by a circuit unit SCH, the second functional unit comprises the test mode detection which consists of a control unit ST and a first and a second voltage-controlled switching element E1 and E2. The switching unit SCH has a first input which is linked to the signal input IN of the integrated circuit IC, and a second input at which a signal MS is available, and a first output line which is linked to the control unit ST, a second output line which is linked to the switching element E1, at which a signal SW1 which is to be tested is available, and a third output line which is linked to the switching element E2, at which a signal SW2 which is to be tested is available. The outputs of the two switching elements E1 and E2 are linked to the node 50. Furthermore, the node 50 is linked to the signal output OUT of the integrated circuit IC and by a wire 5 to the control unit ST. The control unit ST has a first output, at which the signal MS is available, which is linked to a control input of the switching element E1 and to the second input of the circuit unit SCH, and a second output which is linked to a control input of the switching element E2.

The principle of operation of the circuit is explained in the following. In this connection, a differentiation can be made between two operating modes of the integrated circuit.

In the first operating mode, the resistor W1 is separated by the switch T1 from the signal output OUT. As there is thus no potential available at the signal output OUT of the integrated circuit IC that corresponds to the value predefined by the control unit ST, the integrated circuit is not switched into the test mode. Provided that an input signal ES is available at the input pin IN, a derived signal OS is applied to the control unit ST at the first output of the circuit unit SCH. The control unit ST passes the signal on the line 5 unchanged on to the node 50, and thus applies the signal OS as an output signal to the output OUT of the integrated circuit IC.

In the second operating mode, a defined potential is set at the output OUT by means of the switch T1 connecting the resistor W1 to the load element RL, as a result of which the integrated circuit IC is switched into a test mode. A circuit arrangement for potential detection

is illustrated in figure 2. By the switchover into the test mode, a predefined circuit block within the circuit unit SCH, which outputs the signal SW1 to the switching element E1, is selected from the control unit ST by means of the signal MS. Furthermore, the switching element E1 is closed by the signal MS, and the signal SW1 is applied at the signal output OUT as a test signal. The test signal SW1 is an alternating voltage signal in order to minimize the effect on the direct voltage potential at the node 50. If the resistor W1 is separated from the signal output OUT by means of the switch T1, the potential at the node 50 increases to the voltage VDD, and the control unit ST switches the integrated circuit IC back into the normal operating state, that is the signal SW1 is separated from the node 50 by means of the switching element E1, and the selection of the predefined circuit block is cancelled by the signal MS.

The object of the integrated circuit IC shown in figure 2 is to supply an alternating voltage signal in normal operation. Whereas the external wiring of the integrated circuit IC is identical with the embodiment illustrated in figure 1, an advantageous implementation of a control unit ST is presented in a further development of the embodiment in figure 1. In the embodiment illustrated, the switchover of the integrated circuit into the test mode is a function of the result of a logical operation of the set potential value and the control signal of an output stage of the integrated circuit IC. The input IN is linked to a first input of a switching element SCH1 within the integrated circuit IC. Furthermore, the switching element SCH1 has a second input at which a signal MS is available, and a first output at which a signal OS is available which is linked to a node 10, and a second output, at which a first signal S1 which is to be tested is available, which is linked to a non-inverting input of a first amplifier LE1, and a third output, at which a second signal S2, which is to be tested is available, which is linked to a non-inverting input of a second amplifier LE2. Furthermore, the input of a signal output stage AS, for example an impedance amplifier, is still linked to the node 10, and at any one time a first negative input 20 and 30 of an AND logic gate L1 and L2. The output of the signal output stage AS is linked to the node 50, to which are linked, apart from the signal output OUT, a load resistor RL downstream of the voltage VDD and in each case the output of a voltage-controlled switching element E1 and a voltage-controlled switching element E2. Furthermore, a first non-inverting input of a comparator I1 and a first non-inverting input of a comparator I2 are linked to the node 50. A lower threshold voltage V1 is available at the inverting input of the comparator I1, which together with the second upper threshold voltage V2 available at the inverting input of the comparator I2 forms a window discriminator. The output of the comparator I1 is linked to an affirmative input of an AND logic gate L1, the output of the second comparator I2 is linked to a second negative input of an AND logic gate L1. The output of the logic gate L1, at which a signal SE1 is available, is linked to both the control input of a switching element E1 and to the second input of the circuit unit SCH1. Furthermore, the node 50 is linked to a first non-inverting input of a comparator I3 and to a first non-inverting input of a comparator I4. A lower threshold voltage V3 is available at the

inverting input of the comparator I3, which together with the upper threshold voltage V4 available at the inverting input of the comparator I4 forms a second window discriminator. The output of the comparator I3 is linked to an affirmative input of an AND logic gate L2, the output of the comparator I4 is linked to the second negative input of an AND logic gate L2. The outlet of the logic gate L2, at which a signal SE2 is available, is linked to the control input of a load element E2. Furthermore, a reference voltage P1 is available at the inverting input of the amplifier LE1. The output of the amplifier LE1, at which the signal SW1 is available, is linked to the node 50 by means of the voltage-controlled switching element E1. Furthermore, a reference voltage P2 is available at the inverting input of the regulated amplifier LE2. The output of the amplifier LE2, at which the signal SW2 is available, is linked to the node 50 by means of the voltage-controlled switching element E2.

The principle of operation of the integrated circuit IC depending upon the external wiring is described in the following. There are two different operating modes.

In the first operating mode, which represents the normal operating mode, an input signal ES is available at the signal input IN, from which the circuit unit SCH1 derives the input signal OS for the output amplifier AS. As a signal is available at the node 10 and thus at both of the first inputs of the logic gates L1 and L2, the result of the two AND logic operations is "false". The potential of the node 50 is thus not taken into consideration, that is even a potential value set by the resistor W1 would not switch the integrated circuit into the test mode. As a result, both the voltage-controlled switching elements E1 and E2 remain open. The amplified signal OS is available at the signal output OUT, whereby this represents the output signal of the integrated circuit IC in normal operation.

In the second operating mode, there is no signal OS available at the node 10. The integrated circuit IC is thus switched into a test mode by an external wiring, provided that the potential value set at the node 50 lies within the interval of one of the two window discriminators. In the illustrated embodiment, a potential, which lies within the voltage interval given by the first window discriminator, is set at the node 50 by means of the switch T1 connecting the resistor W1 to the load element RL. As the signals only have the correct polarity at the three inputs of the logic gate L1, only the result of the AND logic operation of the logic gate L1 is "true" and the output signal SE1 is switched to "high". At the same time as the switching element E1 closes, a predefined circuit component in the circuit unit SCH1 is selected by the signal SE1, and a signal shape is generated which is applied in the shape of the signal S1 to the node 50 as signal SW1 by the amplifier LE1. The signal SW1 to be tested is thus available at the signal output OUT. If the switch T1 is opened, the potential at the node 50 increases to above the upper limiting value of the first window discriminator, and the output signal SE1 of the logic gate L1 is switched to "low" because the result of its logic operation is now "false". The selection of the predefined circuit component is terminated and the switching element E1

separates the signal SW1 from the node 50. The node 50 is raised to the value of the voltage VDD by the load element RL (pull up) so long as no further signals are fed to the node 50. If the resistor W2 is linked to the signal output OUT by means of the switch T2, a potential appears at the node 50 which lies within the interval of the second window discriminator. Thus only the result of the logic gate L2 is "true", and the test signal SW2 is applied to the signal output OUT by means of the switching element E2. If the resistor W2 is separated, the logic gate L2 separates the test signal SW2 from the signal output OUT by means of the switching element E2, and the potential of the node 50 is raised to the value of the voltage VDD.

So that the two test signals SW1 and SW2 have minimal effect on the prevailing direct voltage value at the node 50, or a coupling with the prevailing other window discriminator does not occur as a result of signals SW1 and SW2 having an excessive alternating voltage amplitude, the signals S1 and S2 are defined by the amplifiers LE1 and LE2 as regards their maximum amplitude as well as the direct voltage offset. In order to achieve the greatest possible amplitude swing, it is advantageous to select the direct voltage offset of the signals SW1 and SW2 so that this lies in the middle of the interval defined by the respective window discriminator. If the respective switching elements E1 and E2 are open, the test signals are only available at the respective inputs of the switching elements E1 and E2.

In contrast to the logic gate L1, the output of the logic gate L2 is exclusively linked to the control input of the switching element E2. Therefore, a selection, that is an activation or deactivation of circuit functions within the circuit unit SCH1, cannot be made with the signal SE2.

Finally, it should be noted that with the new method the number of test signals is limited only by the amplitude values of the test signals and the distances required between the individual voltage values available at the signal output.

CLAIMS

What is claimed is:

1. Method for testing an integrated circuit (IC) which has at least one signal output (OUT) and can be switched into a test mode and which has at least one circuit unit (SCH), **wherein**
   - a potential value is applied at the signal output (OUT) in order to switch into the test mode, and
   - in the test mode a test signal (SW1, SW2) generated by the circuit unit (SCH) is applied at the signal output (OUT).

2. Method in the test mode, according to claim 1, **wherein** the potential value at the signal output (OUT) is generated by means of a passive component, for example a resistor (W1, W2).

3. Method according to claim 1 **wherein**, in the test mode, the circuit unit generates a plurality of test signals (SW1, SW2) which in each case are sent to the signal output (OUT) by applying specific potential values.

4. Method according to claim 2 **wherein**, in the test mode, the circuit unit generates a plurality of test signals (SW1, SW2) which in each case are sent to the signal output (OUT) by applying specific potential values.

5. Method according to claim 4 **wherein** the potential at the signal output (OUT) is compared with a defined reference value (P1, P2, P3, P4) within a first defined time window, and the integrated circuit (IC) is switched into the test mode in a second time window.

6. Method according to claim 5 **wherein** the potential value is applied at the signal output (OUT) and the test signal (SW1, SW2) is output at another signal output.

7. Method according to claim 5 **wherein** the switchover into the test mode is a function of the result of a logical operation, and the logical operation is made between the potential value applied at the signal output (OUT) and a signal (OS) generated by the circuit component (SCH).

8. Method according to claim 2 **wherein** circuit blocks within the circuit unit (SCH) are activated or deactivated with the switchover into the test mode.

9. Method according to claim 7 **wherein** circuit blocks within the circuit unit (SCH) are activated or deactivated with the switchover into the test mode.

10. Method according to claim 2 **wherein** the potential value applied at the signal output (OUT) lies within an interval of a window discriminator.

11. Method according to claim 9 **wherein** the potential value applied at the signal output (OUT) lies within an interval of a window discriminator.

12. Method according to claim 10 **wherein** the signal value of the test signal (SW1, SW2) lies within the voltage interval defined by the window discriminator.

13. Method according to claim 12 **wherein** the signal value of the test signal (SW1, SW2) lies within the voltage interval defined by the window discriminator.

14. Circuit arrangement for performing the method according to one of the claims 1 to 13 with an integrated circuit (IC) which has at least one signal output (OUT), at least one switching element (E1, E2) and at least one circuit unit (SCH),
wherein

- the integrated circuit (IC) has a control unit (ST) which is linked to the signal output (OUT) for testing the potential at the signal output (OUT), and
- the control unit (ST) is linked to at least one switching element (E1, E2), and
- the input of the switching element (E1, E2) is linked to an output of the circuit unit (SCH), and
- the output of the switching element (E1, E2) is linked to the signal output (OUT).

15. Circuit arrangement according to claim 14,
wherein

- the control unit (ST) for adapting the signals to be tested to the potential of the signal output (OUT) contains an amplifier (LE1, LE2), and
- the input of the amplifier (LE1, LE2) is linked to the output of a circuit unit (SCH1),
- the output of the amplifier (LE1, LE2) is linked to the input of the switching element (E1, E2),
- the control unit (ST) contains at least two comparators (I1, I2 and I3, I4) which form a window discriminator,
- and has a logic gate (L1, L2) for performing a logic operation on the test signals (SW1, SW2) and at least one more signal (OS) of the circuit unit (SCH),

- the input of the window discriminator is linked to the signal output (OUT), and
- the output of the window discriminator is linked to the input of a logic gate (L1, L2),
- the output of the logic gate (L1, L2) is linked to the control input of the switching element (E1, E2), and
- the output of at least one logic gate (L1, L2) is also linked to the circuit unit (SCH1) for the selection of defined circuit elements within the circuit unit (SCH1).

ABSTRACT OF THE DISCLOSURE

Method for testing signals of an integrated circuit

In previously known methods for testing internal signals of an integrated circuit, additional output pins were required which, in general, were linked to additional measuring pads within the integrated circuit.

In the new method, the circuit functions are tested by using the output pins at which the output signal is present during normal operation of the integrated circuit. By means of a simple, external connection, with which a defined voltage value is set at the signal output, the integrated circuit is switched by means of an integrated control unit into a test mode in which it applies selected signals, which are to be tested, at the signal output. There is no need for additional internal measuring pads or additional output pins.

Docket # 4284
INV.: Matthias EICHIN et al
Title: Method For Testing an Integrated Circuit

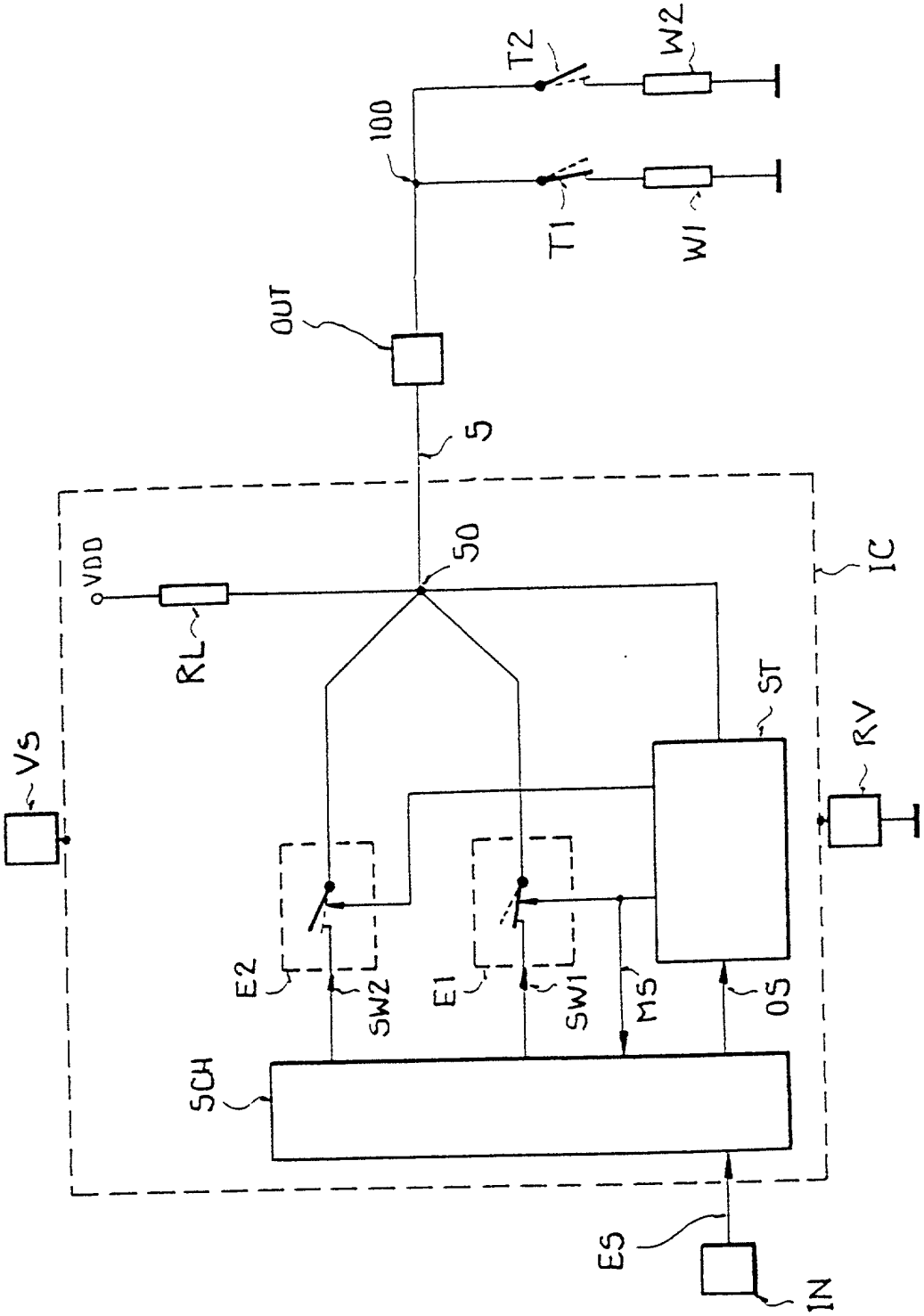

FIG. 1

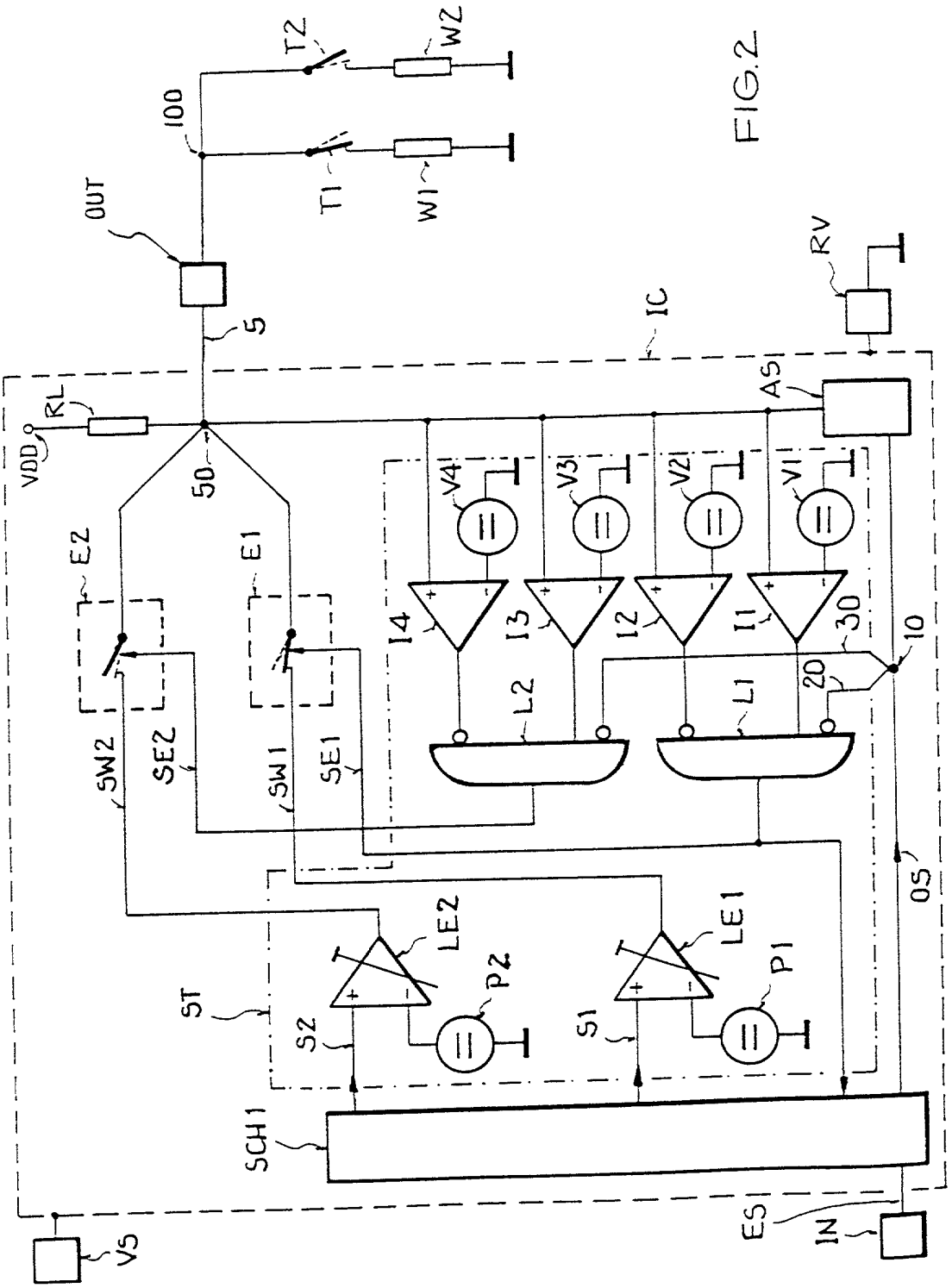

FIG.2

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Declaration and Power of Attorney for Patent Application

Erklärung für Patentanmeldungen mit Vollmacht

German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

daß mein Wohnsitz, meine Postanschrift und meine Staatsangehörigkeit den im nachstehenden nach meinem Namen aufgeführten Angaben entsprechen, daß ich nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent für die Erfindung mit folgendem Titel beantragt wird:

VERFAHREN ZUR PRUEFUNG VON EINER INTEGRIERTEN SCHALTUNG

deren Beschreibung hier beigefügt ist, es sei denn (in diesem Falle Zutreffendes bitte ankreuzen), diese Erfindung

☐ wurde angemeldet am _____ unter der US-Anmeldenummer oder unter der Internationalen Anmeldenummer im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesens (PCT) _____ und am _____ abgeändert (falls zutreffend).

ch bestätige hiermit, daß ich den Inhalt der oben ngegebenen Patentanmeldung, einschließlich der Ansprüche, lie eventuell durch einen oben erwähnten Zusatzantrag bgeändert wurde, durchgesehen und verstanden habe.

ch erkenne meine Pflicht zur Offenbarung jeglicher nformationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 on Belang sind.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR TESTING AN INTEGRATED CIRCUIT

the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

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I hereby claim foreign priority under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

nor Foreign Applications
Frühere auslandische Anmeldungen)

Priority Not Claimed
Priorität nicht beansprucht

100 64 478.3	Fed. Rep. Germany	22/December/2000	☐
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	
			☐
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	

h beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)

h beanspruche hiermit die mir unter Title 35, US-Code, § 120 stehenden Vorteile aller unten aufgeführten US-tentanmeldungen bzw. § 365(c) aller PCT internationalen nmeldungen, welche die Vereinigten Staaten von Amerika nennen, und erkenne, insofern der Gegenstand eines jeden hrigen Anspruchs dieser Patentanmeldung nicht in einer US-tentanmeldung, bzw. PCT internationalen Anmeldung in in einer maß dem ersten Absatz von Title 35, US-Code, § 112 rgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur ffenbarung jeglicher Informationen an, die zur Prüfung der tentfähigkeit in Einklang mit Title 37, Code of Federal gulations, § 1.56 von Belang sind und die im Zeitraum zwischen m Anmeldetag der früheren Patentanmeldung und dem nationalen ler im Rahmen des Vertrags über die Zusammenarbeit auf dem biet des Patentwesen (PCT) gültigen internationalen Anmeldetags kannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)
(Application No.) (Aktenzeichen)	(Filing Date) (Anmeldetag)	(Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)

h erkläre hiermit, daß alle in der vorliegenden Erklärung von mir machten Angaben nach bestem Wissen und Gewissen der Wahrheit entsprechen, und ferner daß ich diese eidesstattliche rklärung in Kenntnis dessen ablege, daß wissentlich und rsatzlich falsche Angaben oder dergleichen gemäß § 1001, Title 3 des US-Code strafbar sind und mit Geldstrafe und/oder efängnis bestraft werden können und daß derartige wissentlich d vorsatzlich falsche Angaben die Rechtswirksamkeit der rliegenden Patentanmeldung oder eines aufgrund deren erteilten tentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

the attorneys and agents associated with U.S.P.T.O Customer No. 21553, and all correspondence should be sent to Customer No. 21553

021553

PATENT AND TRADEMARK OFFICE

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Unterschrift des Erfinders Datum 6.12.01	Inventor's signature Date 6.12.01
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Vor- und Zuname des zweiten Miterfinders (falls zutreffend) Alexander KURZ	Full name of second joint inventor, if any Alexander KURZ
Unterschrift des zweiten Erfinders Datum 05.12.2001	Second Inventor's signature Date 05.12.2001
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D-74025 Heilbronn Bundesrepublik Deutschland	D-74025 Heilbronn Fed. Rep. of Germany

(Im Falle dritter und weiterer Miterfinder sind die entsprechenden Informationen und Unterschriften hinzuzufügen.)

(Supply similar information and signature for third and subsequent joint inventors.)

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